Level-Sensitive Latch Timing Diagrams

Figure 1: RS Latch

The $Q$ (and $\overline{Q}$) output will change if either of the $R$ or $S$ input signals change.

Figure 2: RS Latch w/Enable

The $Q$ (and $\overline{Q}$) output will change if either of the $R$ or $S$ input signals change when the $E$ input signal is high.

Figure 3: Transparent D-Latch

The $Q$ output will change to match the $D$ input signal any time that the $E$ signal is high.
Edge-Sensitive Latch Timing Diagrams

Figure 4: Master/Slave D-Latch (falling-edge triggered)

The $Q$ signal will be set to match that of the $D$ signal whenever a falling edge on $clk$ occurs. (The only thing that can cause the $Q$ output to change is a falling edge on the $clk$ signal line.)