1 Asynchronous Counter

The daisy-chain shown in Fig 1 causes $D_1$ to change in response to $D_0$ changing from high to low which results in $D_1$ changing later than $D_0$. This delay is cumulative as the number of output bits in this type of counter increases. Sometimes this is OK. Other times it is more important that all the outputs change at (or very close to) the same time.

2 Synchronous Counter

In a synchronous counter the state of all the output bits ($D_0$ and $D_1$ in Fig 2) change at the same time in response to the $clk$ signal.

One way to design a circuit that can count synchronously is to determine the next state of each of the output values by using a combinational circuit whose inputs are connected to the current output value signals. The next state signals may then be fed back into the inputs of latches that are used to store the current state of each output signal.

Expressing the next state in the form of a truth table can help illustrate this idea.
Simplifying the output values...

\[ N_1 = (D_1 \land D_0) \lor (D_1 \land \overline{D_0}) \]  
\[ = D_1 \oplus D_0 \]  
\[ N_0 = (D_1 \land \overline{D_0}) \lor (D_1 \land \overline{D_0}) \]  
\[ = (D_1 \lor D_1) \land \overline{D_0} \]  
\[ = 1 \land \overline{D_0} \]  
\[ = \overline{D_0} \]  

We can now add the \( N_0 \) and \( N_1 \) signals to our waveform diagram in Fig 4 and schematic in Fig 5 to see how they are used.

3 Observations

- Synchronous sequential circuits have the clock inputs to all latches connected to the same source-signal.
- Asynchronous sequential circuits have the clock inputs to their latches connected to different (or additional) signals.
- The MSb in a ripple counter changes after the LSb.
Figure 5: Synchronous Counter Schematic

- Given a wide (many bits) enough ripple counter, the MSb can be delayed so long that it is not always obvious which clock cycle is causing it to change!