An 8-Bit Register!
W[0..7] is called a "data BUS"

WA[0..1] is called an "address BUS"

WA[0..1] selects which register we want to write W[0..7] into when WriteEnable is 1.

RA[0..1] selects which register output to 'see' on R[0..7].

R[0..7] is called a "data BUS"

RA[0..1] is called an "address BUS"

WA[0..1] is called an "address BUS"

R[0..7] is called a "data BUS"

W[0..7] is called a "data BUS"

RA[0..1] is called an "address BUS"

R[0..7] is called a "data BUS"
Building a RAM with a bidirectional data bus

- **Bidirectional data bus**
- **Write data bus into RAM when high**
- **Address bus**
- **Put read data onto the bidirectional bus when high**

**Static RAM**

**Tri-state driver.**
Used to ‘disconnect’ the output bus from the SRAM when OE is low.

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Sheet:/tristate/
File:tristate.sch

**Title:** Multiplexing The Data Busses Together

Size: USLetter  Date: 2019-09-18  Rev: 2
KiCad EDA.  kicad 5.1.5+dfsg1-2build2  Id: 3/4
512KB SRAM

Address bus

Bidirectional data bus

Active-low enable and read/write signals

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Sheet: /RAM/
File: RAM.sch

Title: Typical SRAM Chips
Size: USLetter Date: 2019-09-18 Rev: 2
KICad EDA. kicad 5.1.5+dfsg1-2build2 Id: 4/4