Robert Rannie, Northern Illinois University
Milica Kozomara, Texas Instruments

Terms Mainframe Systems Programmers Should Know

Please Note: Memory locations, PSW & Control Block formats, and Names of Control Blocks and Executable System Modules have changed with the Architectural Evolution of the General Purpose Computer (GPC).

The locations, formats, and names presented in this list of "Terms" are based largely on those that were current in the Assist-V (A-V) Environmental Simulator for IBM 360 Systems Software Development. The A-V Simulator incorporates nearly all of the concepts inherent in the GPC.
For further information on A-V, see Part 1 of the "Boot Camp" series and http://www.cs.niu.edu/~rrannie/.

Fixed Storage Locations
- Dual use for first 24 bytes of Memory
- Special Properties of first 4K of Memory
  - Enables Storage of GPR on Interrupt without using a Base Register
  - Enables LPSW instruction in Dispatcher

Program Status Word
- Locations:
  - "OLD PSW" & "NEW PSW" locations are in Memory
  - "Current PSW" refers to a Special "Register", Not Memory
- Keys
  - Key 0
  - Protection Rules: No Fetch Protection
  - Protection Rules: With Fetch Protection
  - S0C4 Abends
- Problem/Supervisor State
- Wait/Run State
- Masks
  - I/O
  - External (including "Timer")
  - Machine Check
  - Program
    - Fixed Point Overflow
    - Decimal Overflow
    - Exponent Underflow
    - Significance

Channels

Channel Status Word

Channel Address Word

Channel Command Words

Interrupts
- Stages
  - Hardware: PSW Swap, Four Steps
  - Software: First Level Interrupt Handler (FLIH),
    - Saving the Essence of the Interrupted Program
- Types
  - External
  - Supervisor Call
  - Program
  - Machine
  - Input/Output
  - (Restart)
- Priorities
- Maskable
  - Yes. If Interrupt occurs while Masked off:
    - Remains pending
      - Doesn't remain pending, it is lost
        - Indicators that Interrupt was lost
  - No. It cannot be Masked off

- Assembly programming
  - Addressing Considerations
    - Address equals summation of:
      - Displacement, and
      - Index (X) GPR, and
      - Base (B) GPR
    - Exception: Built in hardware feature of the GPC
      - When X or B is GPR-Zero,
        - contents of GPR-Zero is ignored!
      - THIS IS THE CRITICALLY
        - NECESSARY BASIS OF THE GPC!
  - Privileged Instructions
    - SSK
    - ISK
    - LPSW
    - SIO
  - S0C2 Abends
    - (Privileged Operation Exception)
  - SVC Instructions
    - Input & Output Parameter Registers
    - Internal Register Use Conventions
  - Branch entries to SVC modules
- Control Blocks
  - Communication Vector Table
    - "TCBWORDS"
  - Task Control Block
  - Request Block
  - Event Control Block
  - Input/Output Block
  - Unit Control Block
  - Request Queue Element
  - SVC Table
- System Modules
  - Initial Program Load
    - I/O Phase
    - Current PSW loading Phase
      - Establishing Addressability, via
        - BALR
      - Setting all 2K memory blocks via
        - SSK,
        - Establish memory size via S0C5
        - Abend
  - Dispatcher
  - First Level Interrupt Handlers
    - External (including "Timer")
    - Supervisor Call
    - Program
    - Input/Output
  - Master Scheduler
  - SVCs 0, 1, 2, 3, 8, 13, 14 and associated Macros